SWITI HTSI
PEF 20451 Version 1.1
SWITI HTSI-L
PEF 20471 Version 1.1
SWITI HTSI-XL
PEF 24471 Version 1.1

Transceivers

Infineon technologies

Never stop thinking.

Edition 2000-06-05

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

SWITI HTSI
PEF 20451 Version 1.1
SWITI HTSI-L
PEF 20471 Version 1.1
SWITI HTSI-XL
PEF 24471 Version 1.1

Transceivers

Never stop thinking.

Revision History: **2000-06-05** DS 1

Previous Version:

Page	Subjects (major changes since last revision)

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

Table of Contents **Page**

Preface

The new switching family SWITI can be used for a wide range of telecommunication and data communication applications. This document provides a basic description of the SWITI HTSI family.

Related Documentation

H.100 Hardware Compatibility Specification: CT Bus, revision 1.0

H.110 Hardware Compatibility Specification: CT Bus, revision 1.0

PCI Specification, revision 2.1, PCI special interest group

Compact PCI Specification—PICMG 2.0, revision 2.1

Compact PCI Hot Swap Specification - PICMG 2.1, revision 1.0

H-MVIP Standard, Release 1.1a, GO-MVIP Inc., January 1997

MVIP-90 Standard, Release 1.1, GO-MVIP Inc., October 1994

SC-Bus Specification, ANSI/VITA 6-1994

Your Comments

We welcome your comments on this document. We are continuously trying improving our documentation. Please send your remarks and suggestions by e-mail to

sc.docu_comments@infineon.com

Please provide in the *subject* of your e-mail:
device name (SWITI HTSI, SWITI HTSI-L, SWITI HTSI-XL), device number (PEF 20451, PEF 20471, PEF 24471), device version (Version 1.1),

and in the *body* of your e-mail:
document type (Product Overview), issue date (2000-06-05) and document revision number (DS 1).

1 Overview

The new Switching IC family, called SWITI, provides a complete and cost-effective solution for all switching systems. The family consists of two sub-families: the HTSI and the MTSI. The Product Overview describes the functionality and characteristics of the HTSI devices, PEF 20451, PEF 20471, PEF 24471.

SWITI devices can be used in today's switching applications such as conventional PBXs and central offices. The HTSI family can also be used in H.100/H.110 applications, which are the key to high performance CTI- and Voice-over-IP-applications, one of the most important future technologies in telecommunications.

The requirements of today's switching applications are met by the following device features:

- Constant delay to support wide band data switching, or channel bundling, for instance
- Bit switching/subchannel switching to support applications such as mobile base stations, DECT, and computer telephony

Additionally, the SWITI family devices provide new features to support a broad range of configurations to ensure adaptability to all switching applications:

- A compliant H.100/H.110 interface (HTSI)
- 8-channel stream-to-stream switching capability (HTSI)
- Message Mode, which allows a preset value to be assigned to any output timeslot
- GPIO (General Purpose I/O) port, controlled from the external microprocessor

SWITI Family ICs

The SWITI family consists of six ICs with different switching capacities. The possible configurations are shown in **Table 1**. The HTSI versions provide an additional H.100 / H.110 interface, while the MTSIs are standard switching devices. The consistent architecture of the SWITI family offers the highest grade of flexibility. Switching performance adaptations in the system can be done only by choosing a device with higher or lower switching capacity. The three MTSI devices can be programmed in the same way as the HTSI devices. Thus all devices of the SWITI family can be operated using one standard SW driver.

Table 1 SWITI Family Tree

Name	Package	Ordering Number	Connections	Local-Bus IN/OUT	H-Bus I/O
HTSI-XL (H-Mode)	P-PBGA-217-1	PEF 24471	2048	16/16	32
HTSI-XL (M-Mode)		PEF 24471		32/32	-
HTSI-L (H-Mode)	P-PBGA-217-1	PEF 20471	1024	16/16	32
HTSI-L (M-Mode)		PEF 20471		32/32	-

Table 1 SWITI Family Tree (cont'd)

Name	Package	Ordering Number	Connections	Local-Bus IN/OUT	H-Bus I/O
HTSI (H-Mode)	P-PBGA-217-1	PEF 20451	512	16/16	32
HTSI (M-Mode)		PEF 20451		32/32	-
MTSI-XL	P-MQFP-100-2	PEF 24470	2048	16/16	-
MTSI-L	P-MQFP-100-2	PEF 20470	1024	16/16	-
MTSI	P-MQFP-100-2	PEF 20450	512	16/16	-

HTSI Devices

The HTSI devices can be operated in two different modes, H-Mode and M-Mode.

In H-Mode, the device offers sixteen local I/Os and a compliant H.100/H.110 interface (32 bidirectional I/Os). All available connections can be assigned as H-bus to H-bus, local bus to local bus connection, or as mixed connections.

In M-Mode, all lines are configured as local I/Os, so that in total 32 local I/Os are provided. Thus, for example, the HTSI-XL device can be used as a 2 k non-blocking switch operating all 32 I/Os at 4 Mbit/s.

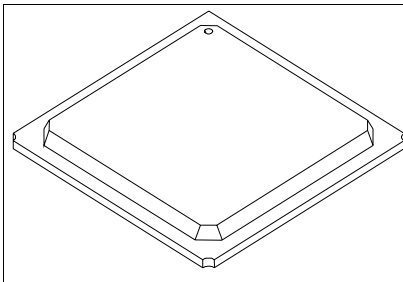
Switching IC
SWITI HTSI

PEF 20451/20471/24471

Version 1.1

CMOS

1.1 Overview of Features



P-PBGA-217-1

General

- Switching capacity of 512, 1024, or up to 2048 connections of different types among different buses
- Programmable data rates of 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s on per stream basis
- Constant delay or minimum delay programmable on per connection basis
- Sub-channel switching ability of 1-bit, 2-bit, 4-bit wide timeslots
- Programmable clock shift for Local Bus
- 8-channel stream-to-stream switching for H.100/H.110 and interoperability bus
- Automatic data rate adaptation
- Optional 8-bit parallel input and/or 8-bit parallel output for first eight lines of Local Bus
- Broadcast capabilities
- Multipoint switching ability
- Read and write access to all timeslots
- Message mode (timeslot write access)
- Programmable framing group
- GPIO port
- 8-bit Microprocessor Interface supports both Intel and Motorola modes
- Optional 16-bit Microprocessor Interface mode (instead of GPIO port)
- On chip PLL for H.100/H.110, SCbus, MVIP, MVIP-H clock operation (master/slave) and for local bus clock operation (master/slave)
- JTAG interface
- Boundary scan according to IEEE 1149.1
- 3.3 V power supply
- 5 V tolerant inputs/outputs

Type	Package
PEF 20451/20471/24471	P-PBGA-217-1

HTSI in H-Mode

- H.100/H.110 compliant interface with all mandatory signals
- Local Bus of up to sixteen PCM ports (16 In/16 Out)
- Hot swapping

HTSI in M-Mode

- Local Bus of up to 32 PCM ports (32 In/32 Out).

1.2 Feature Details

Flexible Data Rates

Each input and output line of the Local Bus is programmable to various data rates. The possible data rates are 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s. Even for the HTSI in M-Mode, all 32 input lines and 32 output lines are configureable, except for the bit rate of 16.384 Mbit/s. In the case of 16.384 Mbit/s, only 24 lines can be used. The possible data rate for the data lines of the H-Bus are 2.048 Mbit/s, 4.096 Mbit/s, and 8.192 Mbit/s.

Constant and Minimum Delay

Independent of the addressed buses, each connection can be determined to be a constant delay or minimum delay connection. Constant delay means that any input timeslot or sub-channel is available on the programmed output after two frames. Minimum delay means that the timeslot or sub-channel appears at the output as soon as possible. The minimum delay depends on the chosen connections and the possible range is between 0 and 2 frames.

Sub-Channel Switching

Each connection can be a 1-bit, 2-bit, 4-bit, or 8-bit connection. Sub-Channel switching is applicable to both the Local Bus and the H-Bus and has a constant delay of 2 frames.

Programmable Clock Shift

The position of Timeslot 0 of each Local Bus input line can be programmed within the timeslot before and after the PFS rising edge in half-clock steps. Also, the position of timeslot 0 of all Local Bus output lines can be programmed within the first timeslot after the PFS rising edge.

8-Channel Stream-to-Stream Switching

This feature offers the possibility to efficiently switch one data stream to another at the same or different data rates without occupying switching memory capacity. It mainly supports interoperability between CT-bus (Computer Telephony) devices such as SCbus and MVIP-90 running at different data rates. It is possible to use up to eight lines from the H.1x0 data lines to establish the connections. Input and output frequency can be configured differently.

Automatic Data Rate Adaptation

Connections are also possible between lines operating at different data rates. The programmer specifies input and output line, timeslot, and, if necessary, the sub-channel.

Parallel Mode

The first eight Local Bus input and output lines can be configured to one parallel input or output port respectively. In serial mode, a timeslot is determined by eight consecutive data clock cycles according to each line. In parallel mode, a timeslot is determined by one data clock cycle according to the first eight lines.

Broadcast

This feature enables distribution of one incoming timeslot to various output timeslots.

Multipoint

Multipoint generates one output timeslot with several input timeslots. Each input timeslot is logically AND or OR connected (selectable) with a constant delay of two frames.

Read Access

The programmer has access to any input timeslot. After issuing an appropriate command, the arrival of the timeslot will be reported by interrupt. The value can be read from a dedicated register. For every read request, the command must be issued again.

Message Mode (Write Access)

This feature allows a constant value to be sent to any given output timeslot.

Framing Group

It is possible to specify up to eight different framing signals of 8 kHz. The position of the rising edge and the pulse width can be programmed for each signal. The reference frame is determined by the PFS signal. The pulse parameters are programmed in half step resolution according to a 16.384 MHz clock.

General Purpose Clocks

All eight GPCLK lines can be configured as individual clock outputs with 8 kHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz and, for test purposes, with the internal frequency or the input frequency of the analog PLL (APLL).

GPIO Port

Each line of the General Purpose Input/Output port can be configured to be either input or output. For an input, an edge causes an interrupt. The outputs can be influenced by write access via the Microprocessor Interface. Thus, it is possible to observe and influence additional signals for the user’s application.

Microprocessor Interface

All devices provide a standard 8-bit Microprocessor Interface operating in either Intel or Motorola mode. Optionally, it is possible to configure the GPIO port as additional data lines to provide a 16-bit Microprocessor Interface. The use of the 16-bit Microprocessor Interface reduces the number of write cycles required to configure a connection from seven (in the case of the 8-bit Microprocessor Interface) to three write cycles.

Input/Output Tolerance

The HTSI can be used in a 5 V environment with two additional 5 V (VDD) power supply pins. Inputs and outputs are 5 V tolerant. The outputs have TTL level driving capability. The H-Bus lines of the HTSI can be used in a 3.3 V signaling PCI environment.

1.3 Logic Symbol

The HTSI is dedicated to perform timeslot switching between the Local Bus and the H-Bus or to offer a solution for applications with a high number of local I/Os. The HTSI operates in two modes. In H-Mode (**Figure 1**), it works with the H-Bus. In M-Mode (**Figure 2**), it operates without the H-Bus.
The HTSI in H-Mode provides 16 PCM input lines and 16 PCM output lines and the complete H-Bus with 32 bidirectional H.100/H.110 data lines.

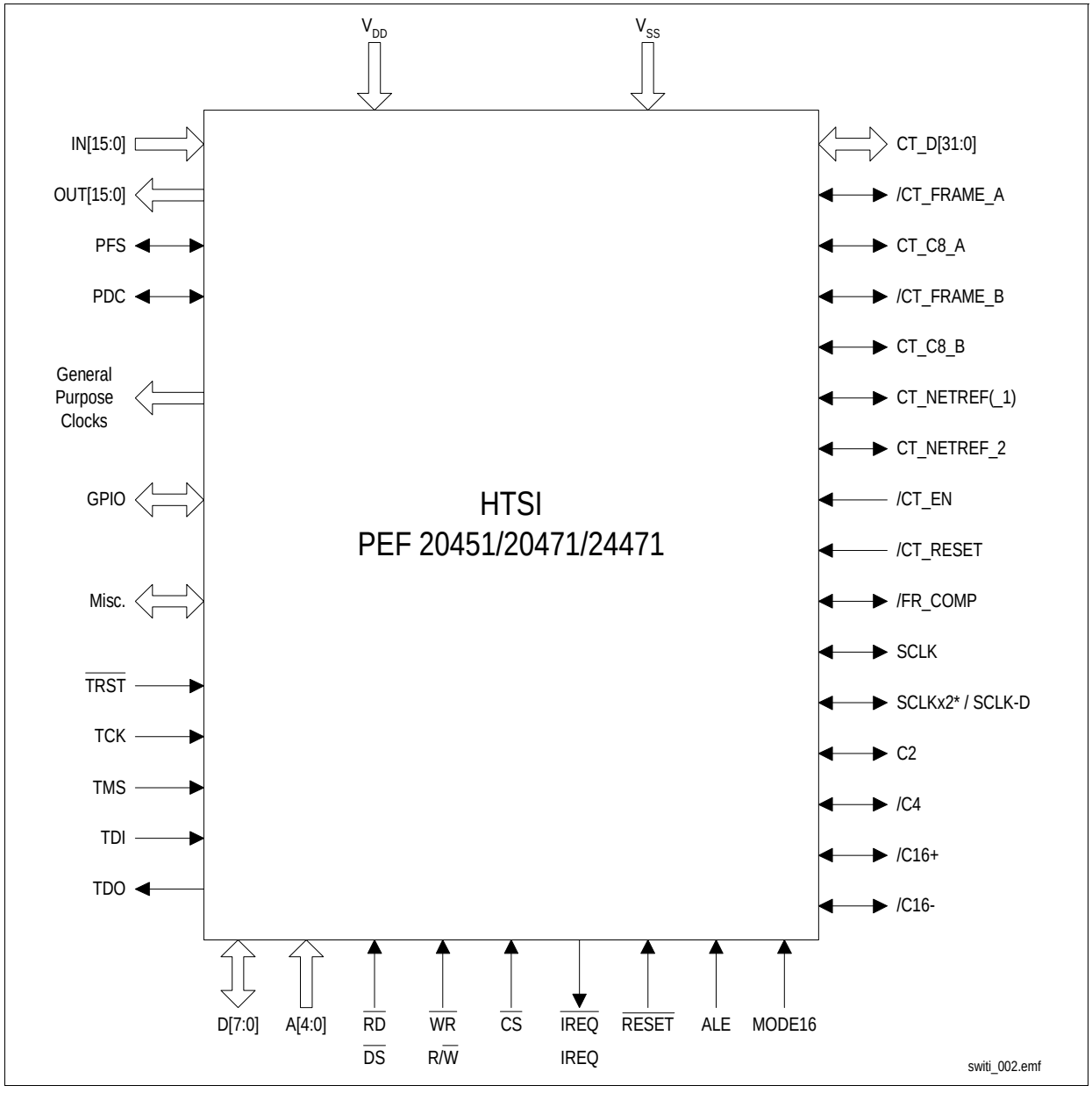


Figure 1 Logic Symbol: HTSI in H-Mode

If no H-Bus is needed, it is possible to configure the HTSI in M-Mode. In this mode, the HTSI provides 32 PCM input lines and 32 PCM output lines.

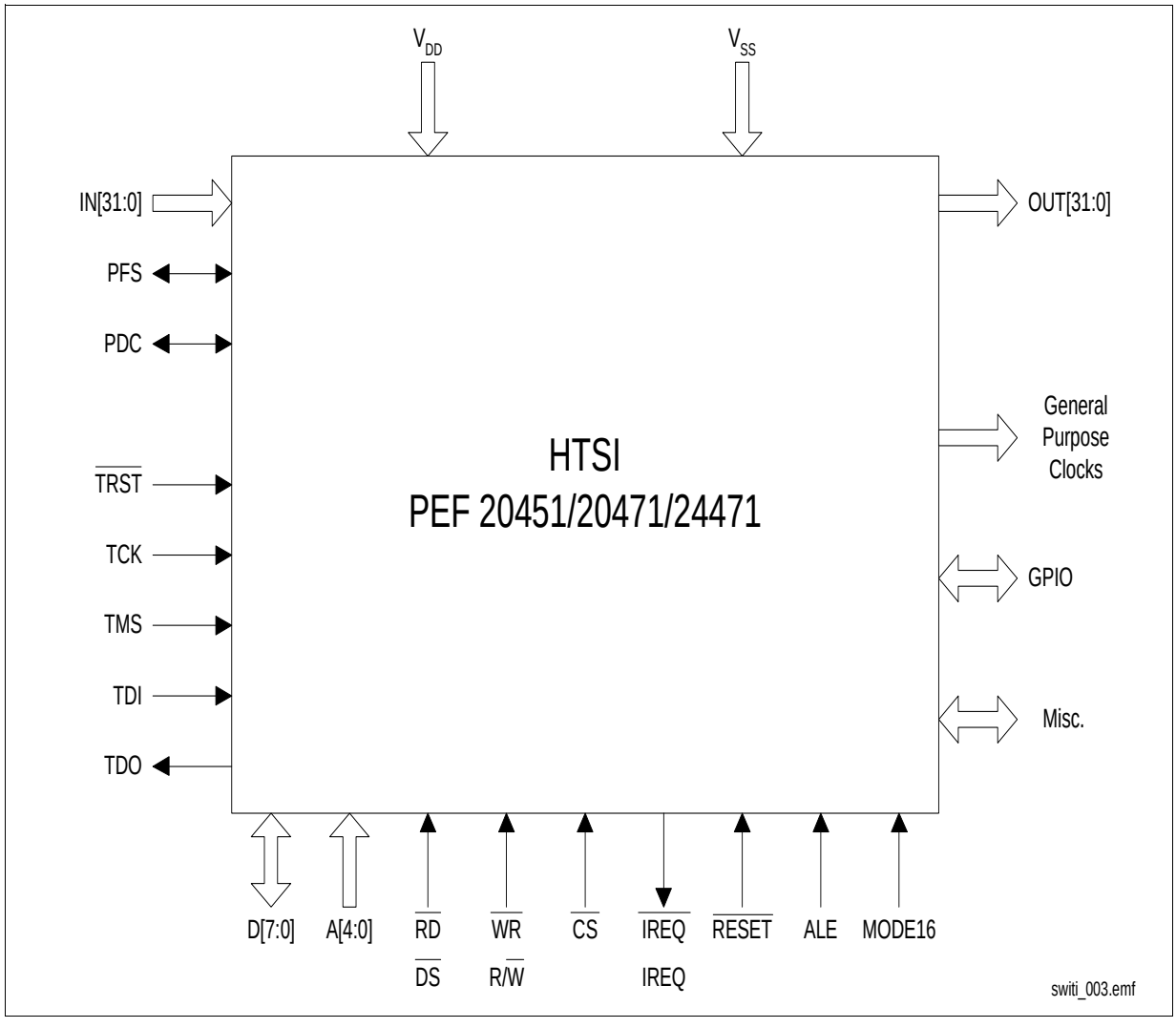


Figure 2 Logic Symbol: HTSI in M-Mode

1.4 Typical Applications

Typical applications of the SWITI HTSI family are:

- PCM switch, concentrator or multiplexer in PBXs, COs, or mobile base stations
- H.100/H.110 interface in
  - Computer telephony systems
  - Internet telephony systems
  - LAN/WAN access devices
  - Enhanced service platforms

The following sections give a general overview of the system integration of the SWITI HTSI family.

1.4.1 Standard PBX or CO Application

The MTSI, or the HTSI in M-Mode, can be used, just as the MTSC or MTSL, in standard Private Branch eXchange or Central Office applications (**Figure 3**), such as in the switching network.

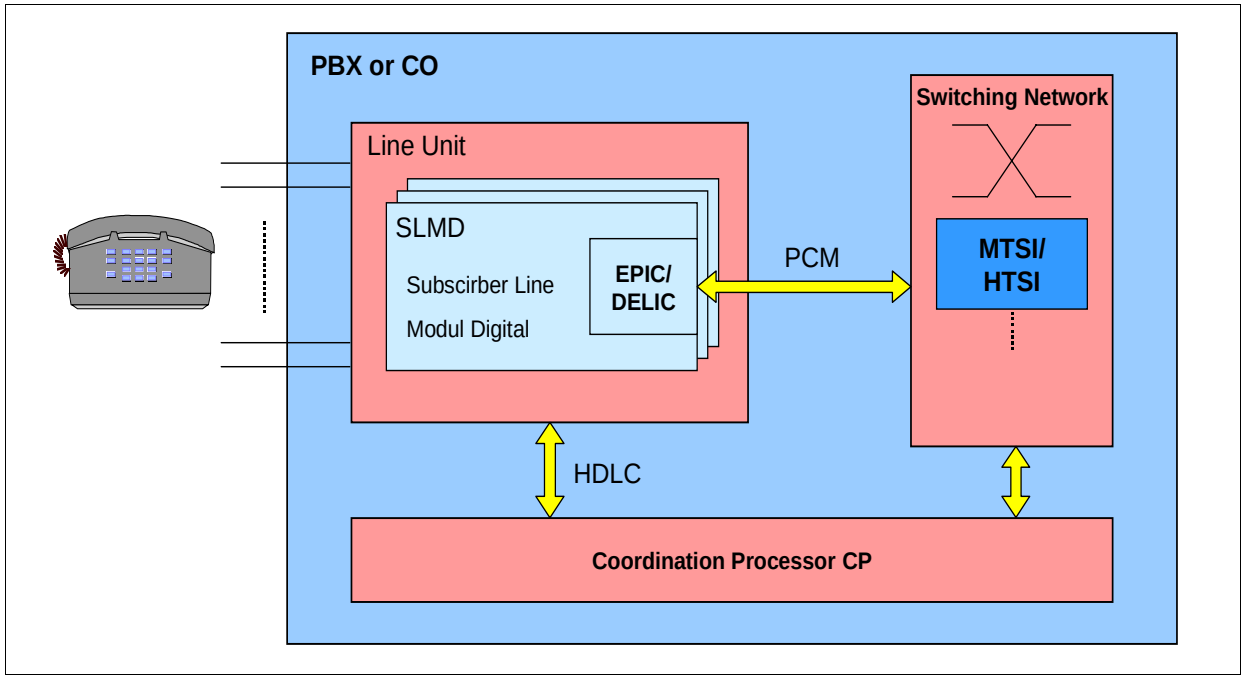


Figure 3 Standard PBX or CO Application

1.4.2 Computer Telephony Application

In Computer Telephony Integration (CTI) applications, resources such as the analog telephone linecards, ISDN ports, switching controllers, FAX firmware, or voice processing modules take the form of plug-in cards in the ISA or PCI slots of a PC. Resource sharing is established by connecting the top of the plug-in cards with cables. This Time Division Multiplex (TDM) bus has evolved from the original H-MVIP, MVIP-90, Dialogic's SC-Bus, into the latest H.100/H.110 bus or H-Bus developed by the Enterprise Computer Telephony Forum (ECTF). By connecting to the H.100/H.110 interface devices, system modules may send and receive data to and from any one of the 4096 TDM timeslots of the H-Bus. The H-Bus also offers the ideal solution for routers to provide a bridge between the data communication and telecommunications system modules.

In Computer Telephony (CT) environment, resource sharing is accomplished by passing data back and forth through the H.100/H.110 bus. **Figure 4** shows an example.

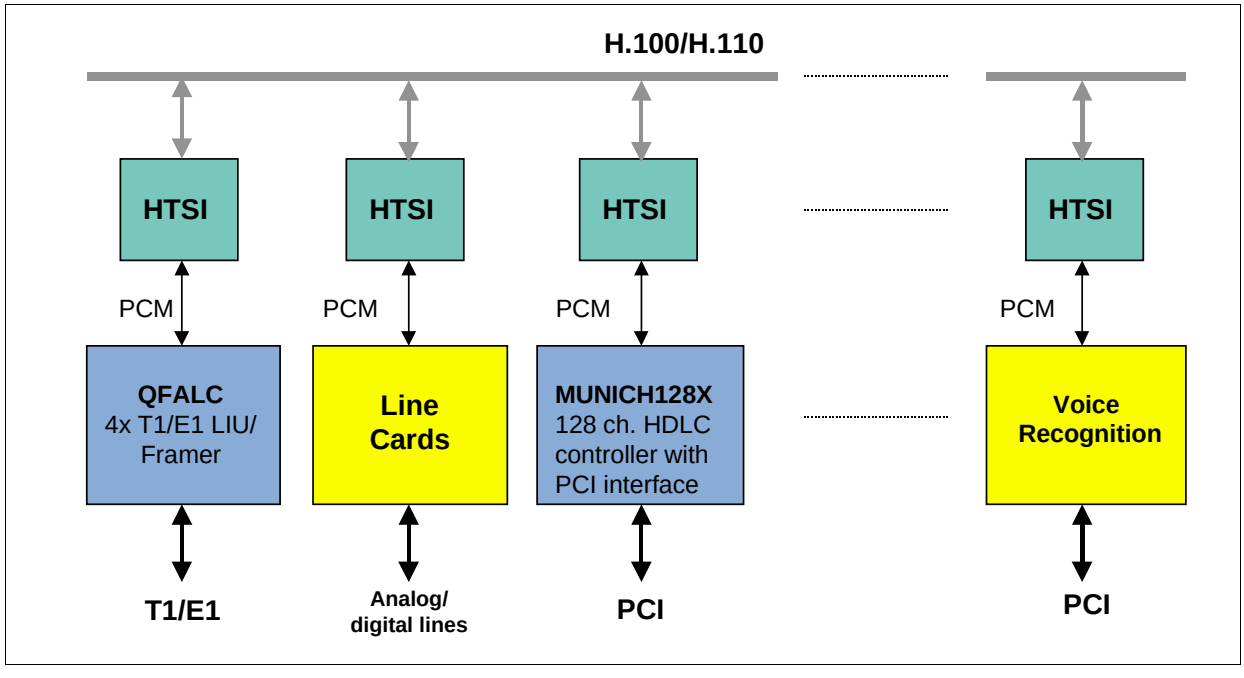


Figure 4 CT Application

1.4.3 Router/Remote Access Application

The HTSI in H-Mode (or the MTSI if no H-Bus interface is used in the system) is used in multivoice applications as the bridge connecting the data communication modules to the telecommunications modules in a router/remote access design. **Figure 5** shows an example.

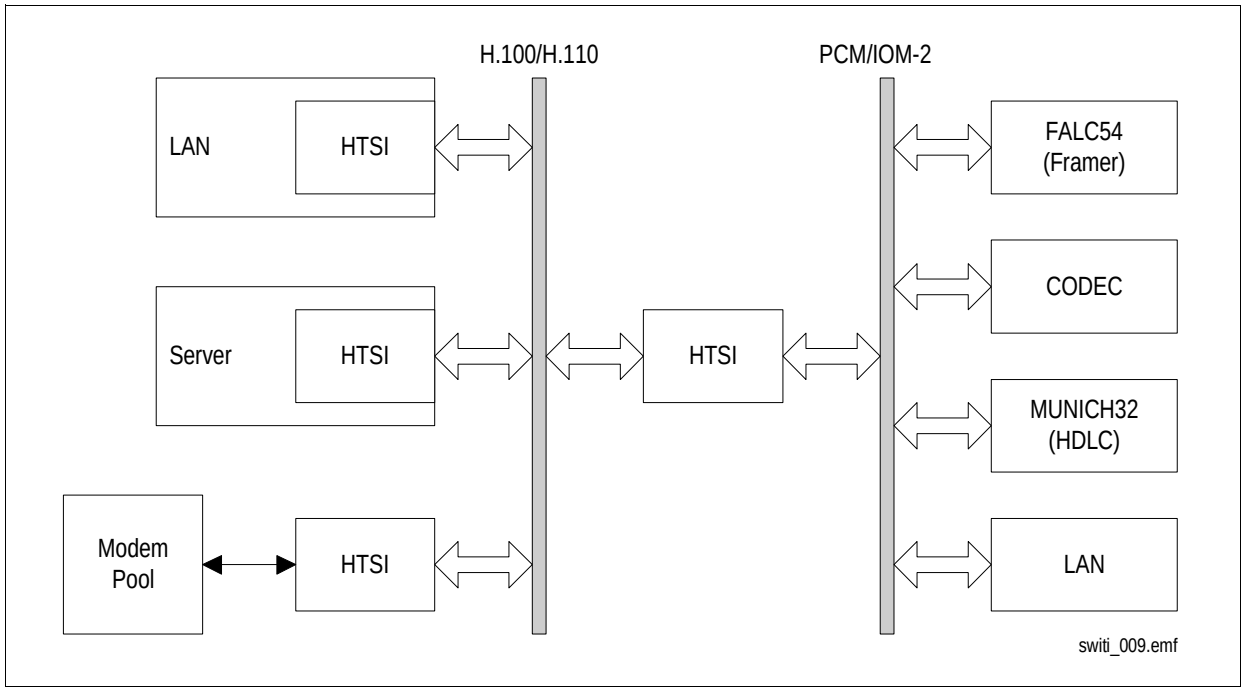


Figure 5 Router / Remote Access Applications

1.4.4 Voice over IP Application

In a Voice over IP application (**Figure 6**), the HTSI (in H-Mode) may be used to connect a conventional PBX to the H-Bus. A Vocoder card, also connected to the H-Bus, performs speech compression and decompression, whereas an Ethernet card transmits and receives the compressed data over the network.

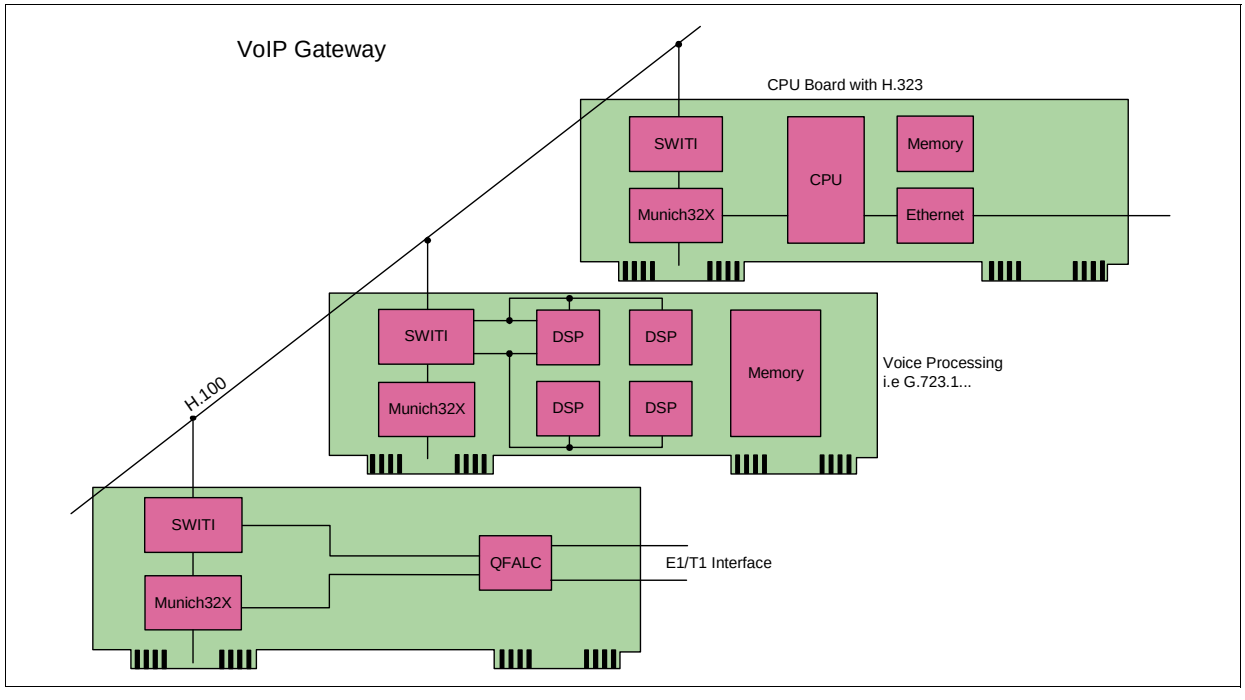


Figure 6 Voice over IP Application

2 Pin Descriptions

The pin descriptions provide overview information with the pin numbers, names, direction, position, and function ordered by the various interfaces.

2.1 Pin Diagram

P-BGA-217-1

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC	NC	CT_D_0/ IN_16	CT_D_2/ IN_18	IN_3	IN_5	VSS	CT_D_6/ IN_22	CT_D_7/ IN_23	CT_D_8/ IN_24	IN_9	IN_11	VDD	CT_D_12 / IN_28	CT_D_14 / IN_30	NC	NC	A
NC	VSS	VDD	IN_1	VDD5	CT_D_3/ IN_19	CT_D_5/ IN_21	IN_6	IN_7	VDD5	CT_D_9 / IN_25	CT_D_11 / IN_27	IN_12	IN_14	NC	VSS	NC	B
GPCLK_2	NC	VSS	VSS	IN_2	VSS	IN_4	VDD	IN_8	VSS	CT_D_10 / IN_26	VSS	CT_D_13 / IN_29	CT_D_15 / IN_31	VSS	VDD	WR R/W	C
VDD	/CT_ FRAME_A	GPCLK_0	VSS	IN_0	CT_D_1/ IN_17	CT_D_4/ IN_20	VDD	VSS	VDD	IN_10	IN_13	IN_15	VSS	VSS	C2	A_1	D
GPCLK_5	VSS	GPCLK_ 3	GPCLK_1										RD/DS	A_0	A_2	VDD	E
GPCLK_7	GPCLK_6	CT_C8_A	GPCLK_4										ALE	/C4	VSS	/C16+	F
VSSA	VDDA	/CT_ FRAME_B	CT_C8_B										A_4	A_3	D_0	D_2	G
ECLKO	M-MODE	CT_ NETREF_2	VDD										VDD	D_1	D_3	/C16-	H
ECLKI	RESERV.	RESERV.	VSS										VSS	D_4	VDD	VSS	J
H110- MODE	/CT_ RESET	NTWK_2	VDD										VDD	D_6	/FR_ COMP	D_5	K
NTWK_1	VDD	RESET	IREQ										GPIO_1	SCLK	GPIO_0	D_7	L
VSS	MODE16	VDD	CT_ NETREF_1										GPIO_5	GPIO_3	VSS	VDD	M
CS	VSS	PFS	TDO										VDD	GPIO_6	SCLKX2* SCLK-D	GPIO_2	N
PDC	TRST	TMS	VSS	VSS	CT_D_17/ OUT_17	CT_D20/ OUT20	VDD	VSS	VDD	OUT_10	OUT_13	CT_D_30/ OUT_30	VSS	VSS	GPIO_7	GPIO_4	P
TDI	TCK	VSS	VDD	OUT_1	VDD5	OUT_4	VDD	CT_D22/ OUT22	VSS	CT_D_26 / OUT_26	VDD	CT_D_28/ OUT_28	OUT_15	VSS	NC	/CT_EN	R
NC	VSS	NC	CT_D_16/ OUT_16	CT_D_18/ OUT_18	OUT_3	OUT_5	VSS	CT_D_23/ OUT_23	CT_D_24/ OUT_24	OUT_9	OUT_11	VSS	CT_D_29/ OUT_29	CT_D_31/ OUT_31	VSS	NC	T
NC	NC	OUT_0	OUT_2	VSS	CT_D_19/ OUT_19	CT_D_21/ OUT_21	OUT_6	OUT_7	OUT_8	VDD5	CT_D_25/ OUT_25	CT_D_27/ OUT_27	OUT_12	OUT_14	NC	NC	U

P-BGA- 217-1

VSS	VSS	VSS
VSS	VSS	VSS
VSS	VSS	VSS

Bottom View

switi_076.emf

Figure 7 Pin Configuration

3 Architectural Description

The following sections give a short overview of the functionality of the SWITI.

3.1 Functional Block Diagram

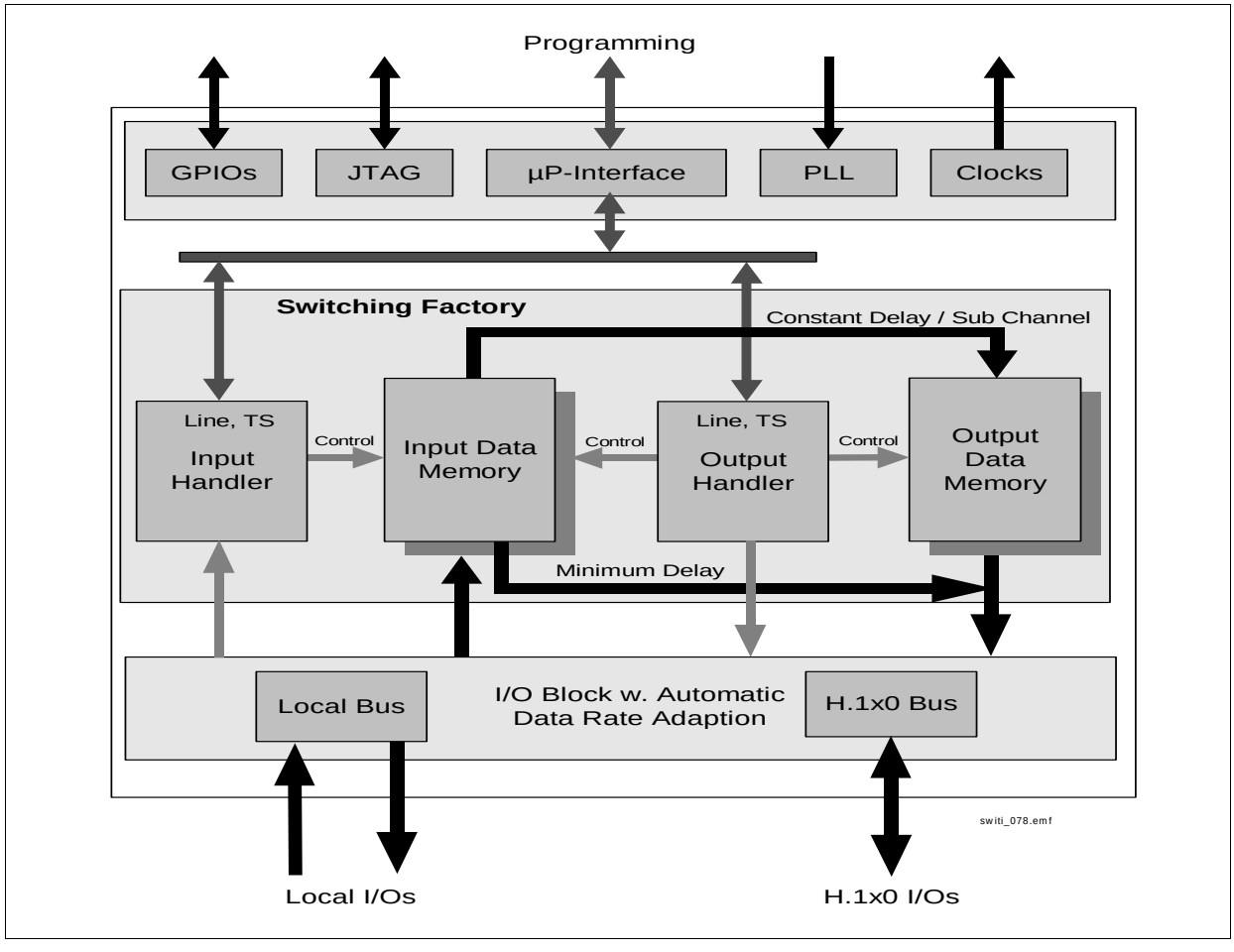


Figure 8 Block Diagram

3.2 Overview of Functional Blocks

Switching Factory

The switching factory is responsible for transferring and handling the incoming data streams to the assigned output channels and time-slots. The block includes a 512, 1024, or 2048 byte input and output data memory as far as an input and output connection memory.

Local-Bus and H-Bus I/O Block

The block is designed to handle the conversion of the data provided via the switching block and the external PCM and H.1x0 interface. It performs the PCM and H.1x0 timing, the data rate selection and the tristate control.

Microprocessor Interface Block

A standard 8-bit multiplexed or de-multiplexed µP interface is provided, compatible to Intel/Infineon Tech. (e.g. 80386EX, C166) and Motorola (e.g. 68040, 68340, 68360, 801) bus systems. If the GPIO port is not needed it can be used to provide a 16-bit µP interface.

GPIO Block

This block supports up to 8 external port lines each one configureable as input or output. A change on an input line may cause an interrupt (if not masked). The user has access to the port configuration and information via the appropriate registers of the µP interface.

PLL and Clock Block

The PLL generates all frequencies supporting the H.1x0, SCbus, MVIP, H-MVIP busses. The internal phase-locked loop (PLL) generates all bus frequencies synchronized to a selected reference signal. The output frequency tolerance is equal to the input frequency tolerance. The PLL operates from a 16.384 MHz, or 32.768 MHz external crystal, oscillator. According to the H.1x0 specification the input frequency tolerance must be ±32 ppm or less.

3.3 Clock Fallback

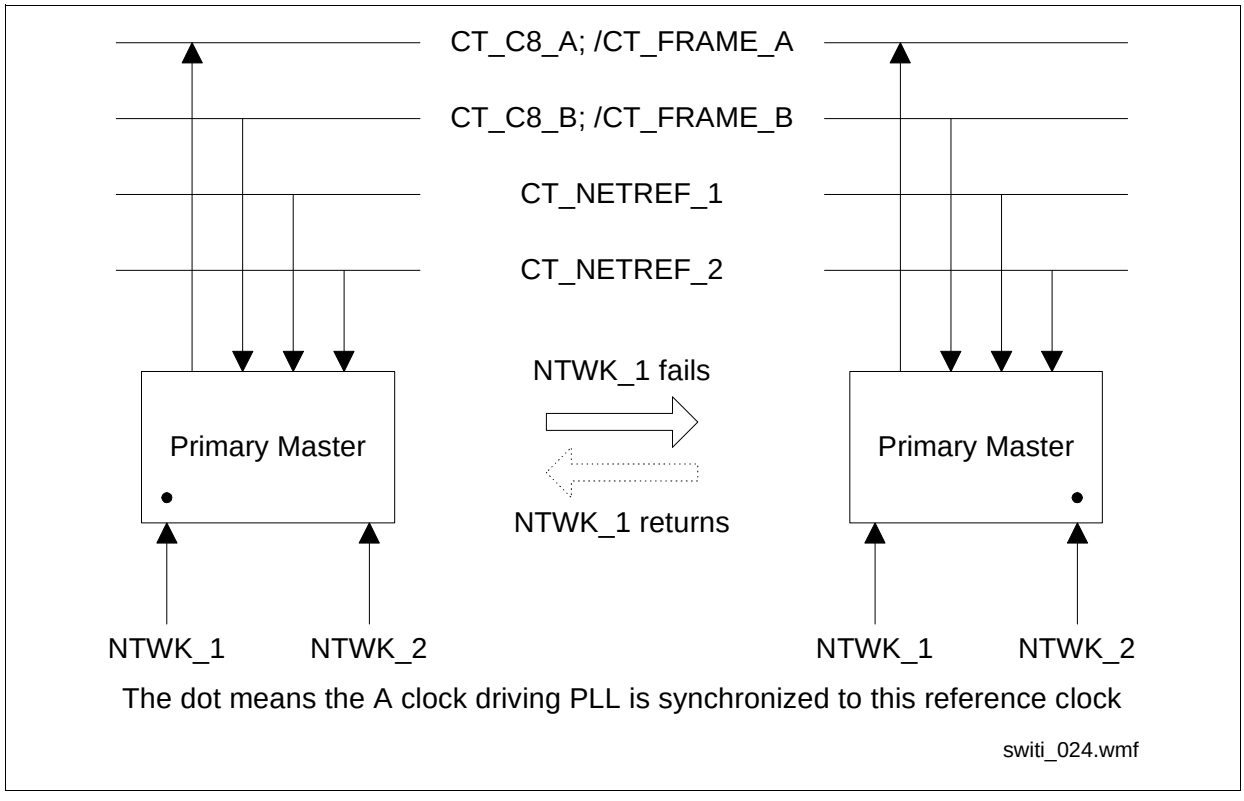


Figure 9 Clock Fallback of Primary Master

The primary master is synchronized to a reference clock (NTWK or CT_NETREF) and drives the CT_C8_A and /CT_FRAME_A clocks. **Figure 9** shows a configuration example. If the primary network reference clock (NTWK_1) fails the device automatically synchronizes to the secondary network reference clock (NTWK_2). If the primary reference clock returns the device may synchronize to it again automatically or by software command (depends on configuration). If not masked the failure is reported by an interrupt.

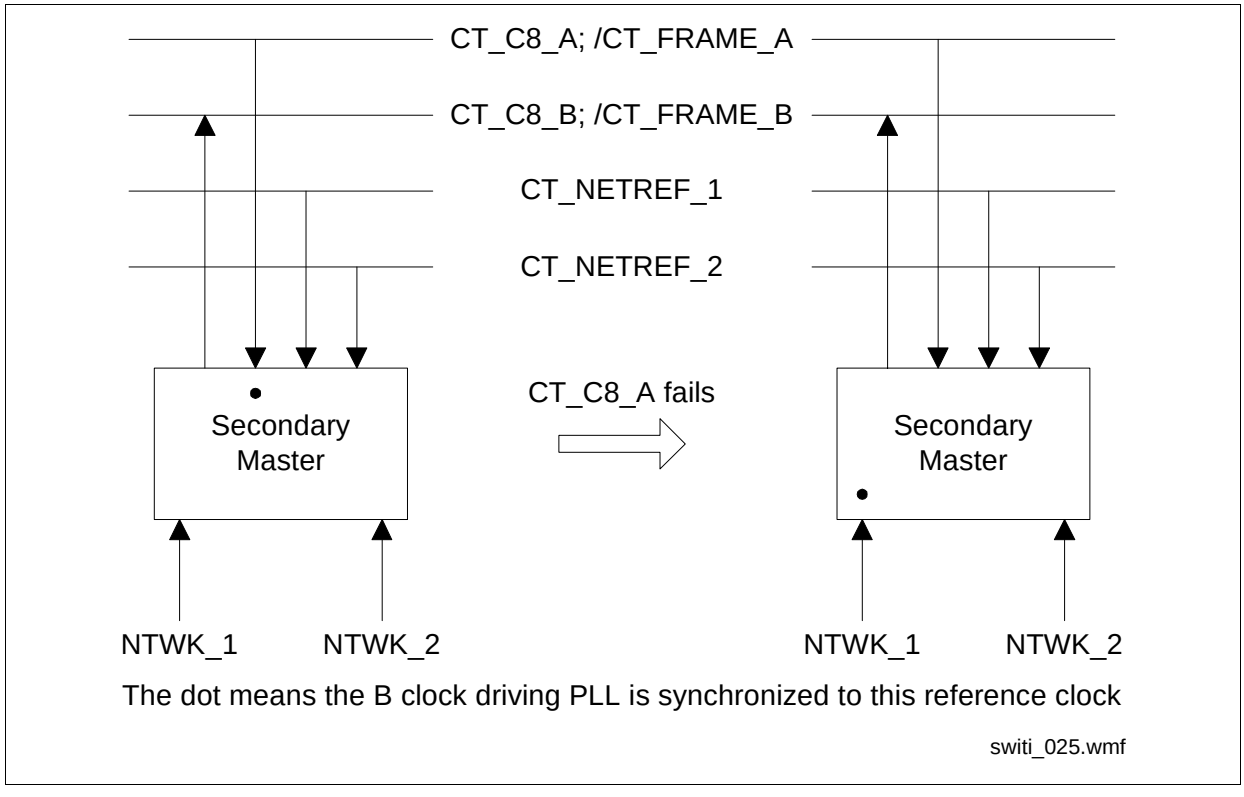


Figure 10 Clock Fallback of Secondary Master

The secondary master is synchronized to CT_C8_A, CT_FRAME_A and drives CT_C8_B and CT_FRAME_B. If one of the CT_A clocks fail the device may synchronize automatically or by software command (depends on configuration) to another reference clock (NTWK or CT_NETREF). **Figure 10** shows a configuration example. If not masked the failure is reported by interrupt.

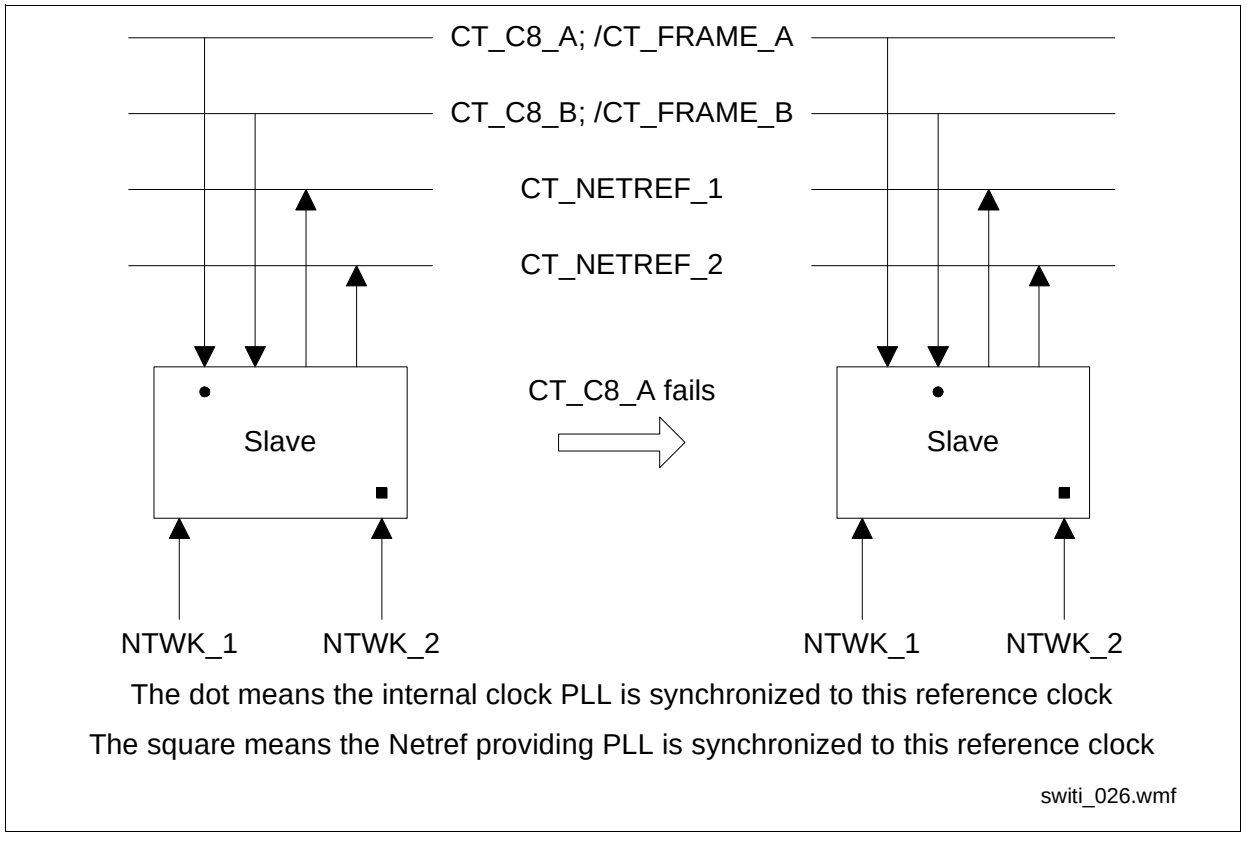


Figure 11 Clock Fallback of Slave

The slave is synchronized to CT_C8_A and CT_FRAME_A. If the clock fails the slave synchronizes automatically or by software command to CT_C8_B and CT_FRAME_B. If not masked the failure is reported by interrupt. If the automatic fallback was issued it must be programmed again.

4 Description of Interfaces

4.1 Local Bus Interface (PCM)

The local bus is a PCM interface consisting of input and output data lines (IN, OUT), a PCM data clock PDC and a frame synchronization signal PFS.

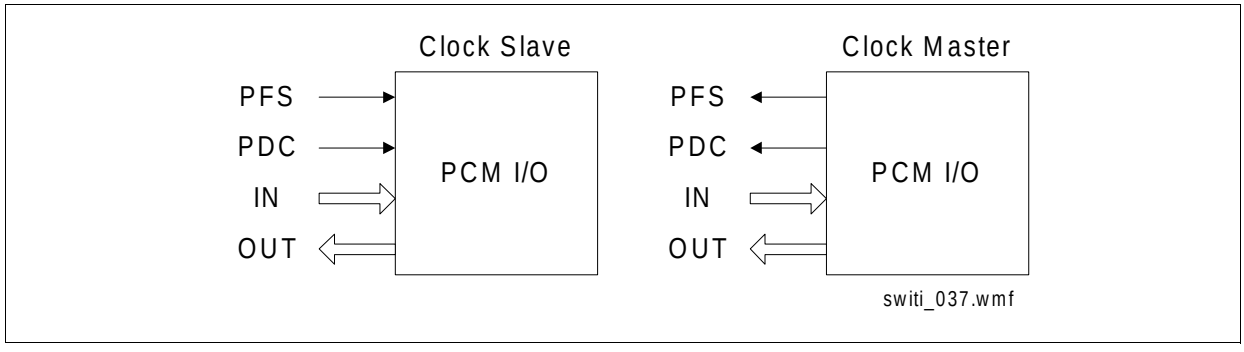


Figure 12 PCM Interface Configurations

The **PFS Frame Sync** is a 8 kHz signal and delimiting the frame. This input signal is used by the SWITI HTSI to determine the start of a frame. A frame is divided into 8-bit wide time slots. The amount of time slots within a frame depends on the selected data rate of PDC which can be 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, 16.384 Mbit/s. The PFS input has a Schmitt-Trigger characteristic.

The **PDC Data Clock** input supply the SWITI HTSI with a data clock. It can be operated with a 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz data rate clock depending on the selected **highest** data mode. The PDC clock signal must be equal or higher as the highest data rate The PDC input has a Schmitt-Trigger characteristic.

A clock slave **must** receive PFS and PDC whereas a clock master drives these signals. To enable or disable the signals for the clock master the command ’PCM Clock Input/ Output Selection’ must be issued.

The time slots are transmitted and received via 16 input and 16 output lines **(IN[15:0], OUT[15:0])**. The input lines have a Schmitt-Trigger characteristic. The output lines have tristate outputs with push-pull characteristic. For every time slot not participating to a connection the output is high impedance.

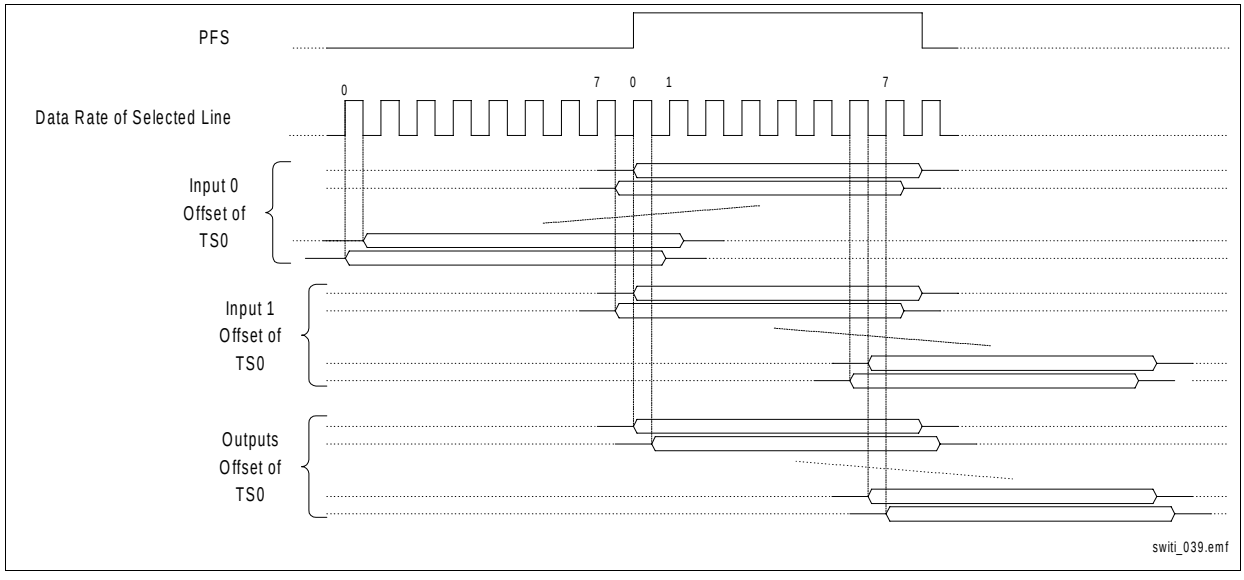


Figure 13 PCM Bit Shifting

For **each** PCM input line the offset of time-slot zero can be adjusted in a range from 0 to 7 bit in half clock resolution before or after the PFS rising edge. For **all** output lines the offset of time-slot zero can be adjusted in a range from 0 to 7 bit in half clock resolution after the PFS rising edge.

The resolution depends on the selected data rate that means the resolution doesn't depend on the PDC signal.

After the reset process the bit shift is disabled for all lines. That means the time-slot 0 starts with the rising edge of PFS. All input data will be sampled with falling edge of the selected data rate and the output data are valid with the rising edge of the selected data rate.

4.2 H-Bus Interface

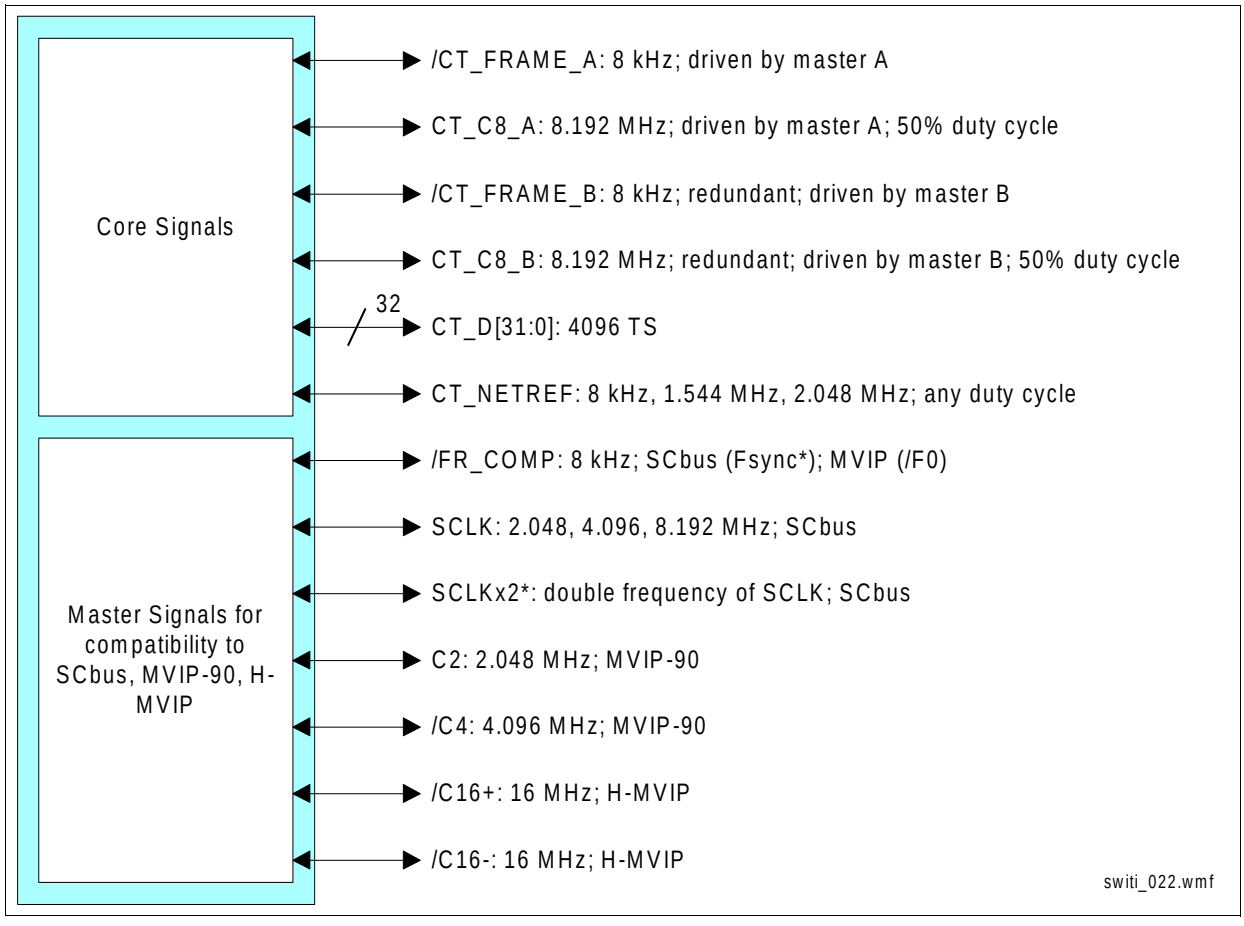


Figure 14 H-Bus Interface in H.100 Mode

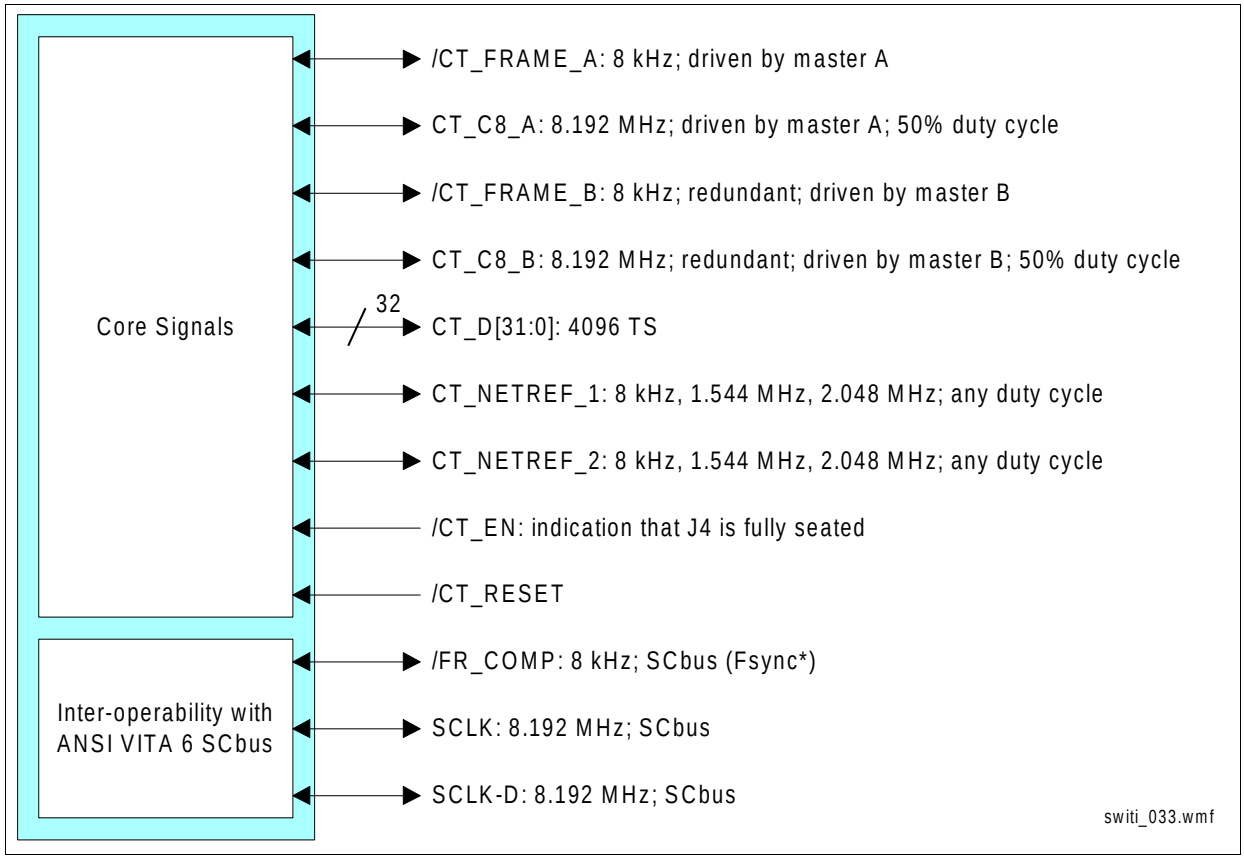


Figure 15 H-Bus Interface in H.110 Mode

The frequency of SCLK in H.110 mode is 8.192 MHz only.

4.3 General Purpose Port (GPIO)

This port consists of 8 lines each one configureable as input or output. A change on an input line may cause an interrupt (if not masked). The user has access to the port configuration and information via the appropriate registers of the µP interface.

Figure 16 shows an example.

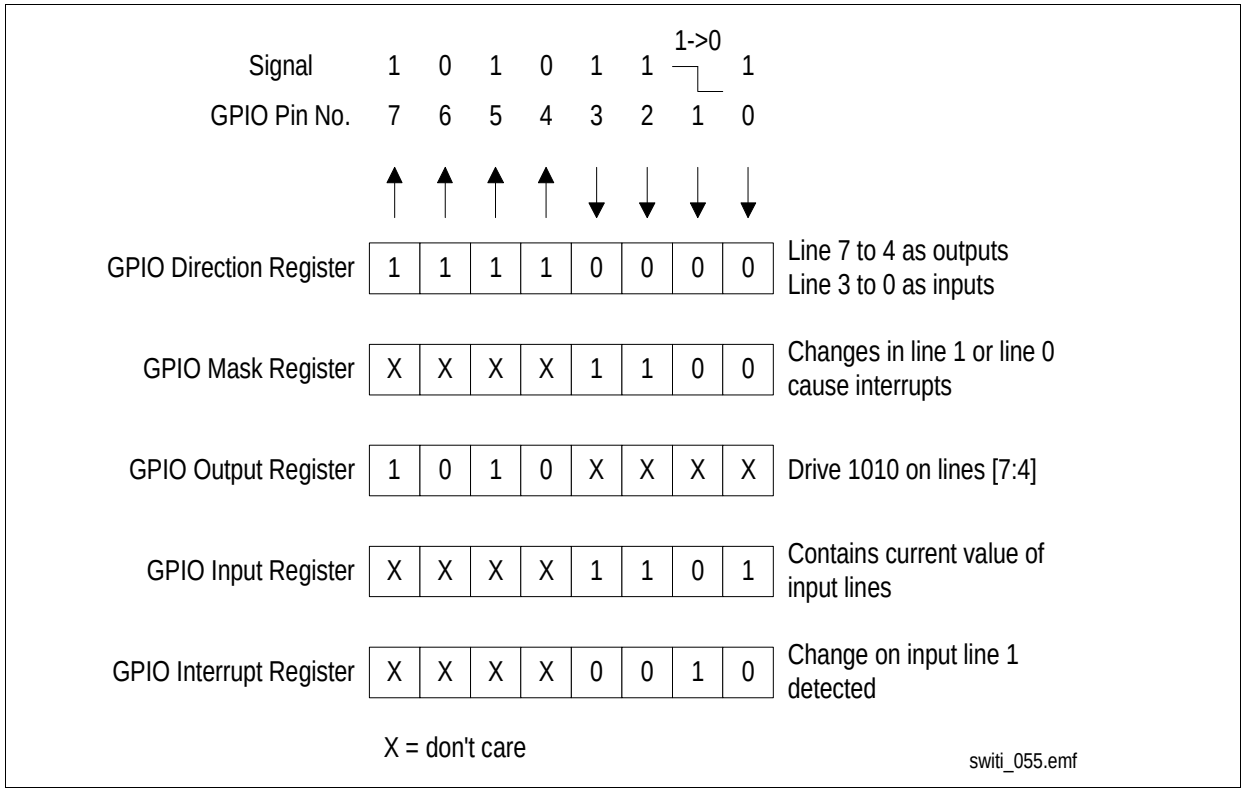


Figure 16 GPIO Port Configuration Example

5 Programming the Device

The register set consists of parameter registers, command registers and status registers. Before issuing a command the parameter registers have to be written accordingly. A connection command can only be issued if the connection command register is ready to be written to (see **Figure 17**).

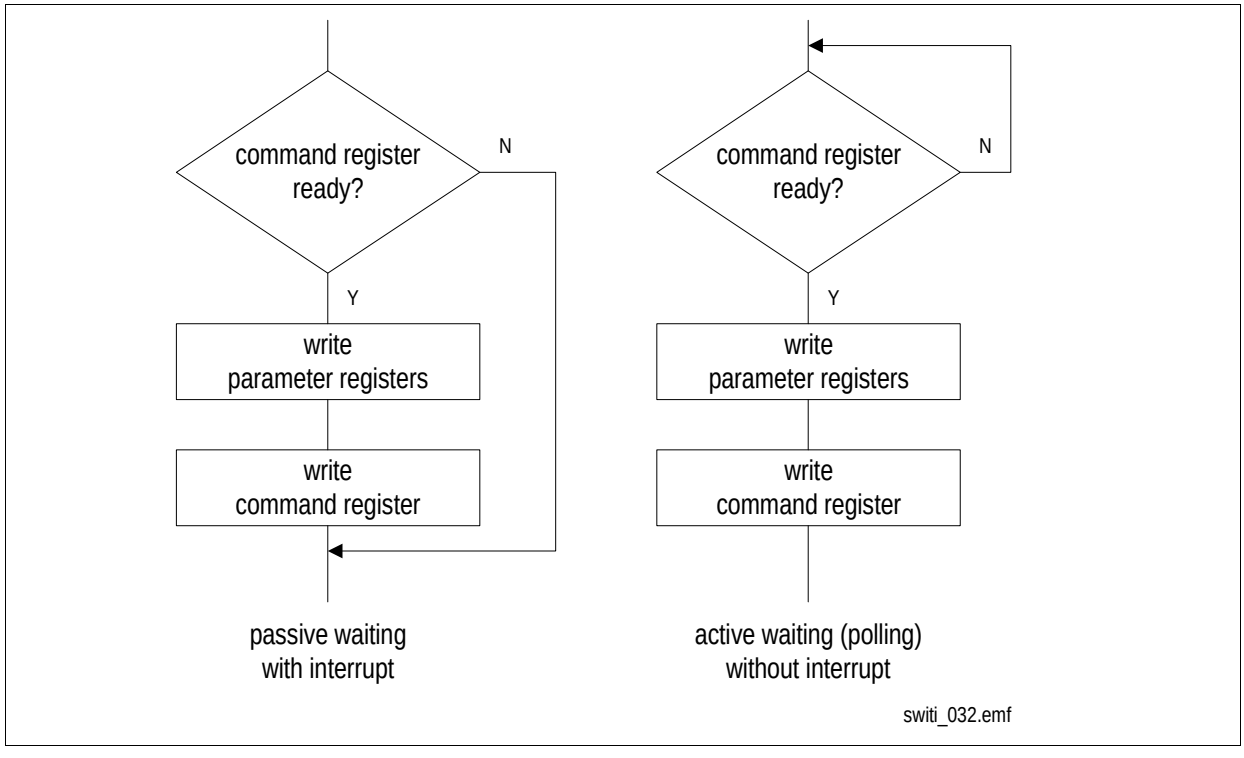


Figure 17 Order of Register Access

5.1 Interrupt Handling

The SWITI HTSI interrupt concept consists of four interrupt status register with their corresponding mask register. The five interrupt status register can be divided in one main register, and two error interrupt register, one general purpose interrupt register and one time slot value register. Every secondary status register and the time slot value register has a bit in the main register to indicate the set of an interrupt in the assigned error or general purpose register or to indicate a new value in the time slot value register.

The interrupt status register can be read via the microprocessor interface. The NFC and RDY will be set and reset from the internal controller. If the GPIO, TSA, ER2, or ER1 is set, the assigned secondary interrupt status register or time slot value register must be read first. After an secondary status register read access, the error status register and corresponding bits in the main interrupt status register will be reset.

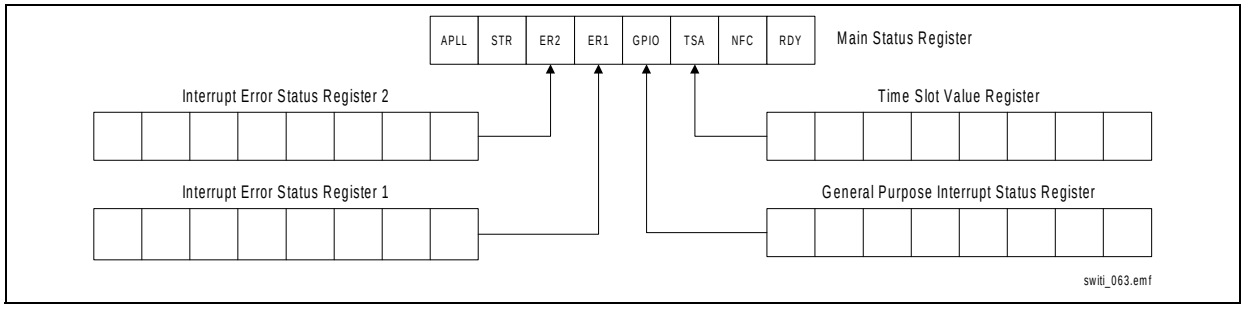


Figure 18 8-bit µP Access Interrupt Structure

Interrupt Structure for a 16-bit Microprocessor Access

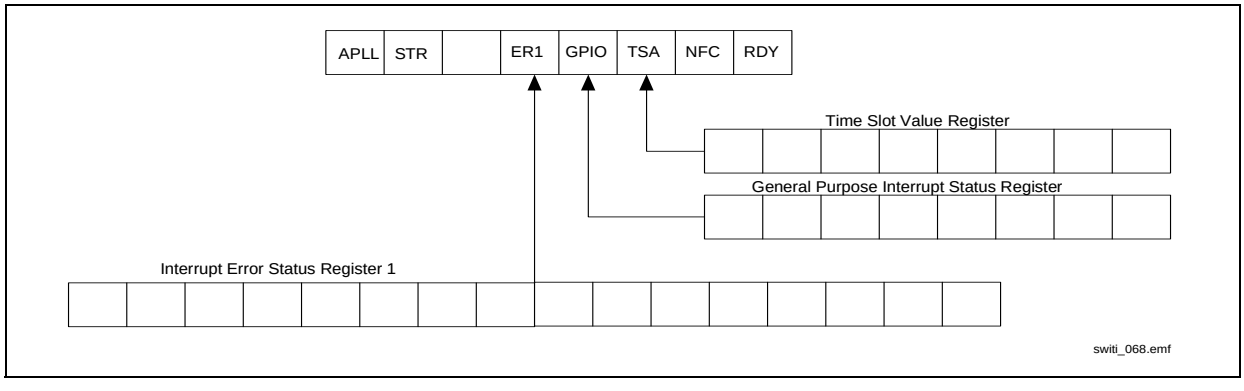


Figure 19 16-bit µP Access Interrupt Structure

In opposite to the 16-bit µP access there is only one bit (ER1) to indicate a change in the 16-bit Interrupt Error Status Register 1.

5.2 Command and Register Overview

The following table (**Table 2**) shows which parameter registers are considered by issuing an appropriate connection command.

Table 2 Affected Registers for Connection Commands

Command	Registers								
	SPA	ITSA	SCA	DPA	OTSA	MV	GI1	GI2	CON
Connect/Disconnect (without subchannels)	x	x		x	x				
Connect/Disconnect (with subchannels)	x	x	x	x	x				
Send Message (without subchannels)				x	x	x			
Send Message (with subchannels)			x	x	x	x			
Stop Message (without subchannels)				x	x				
Stop Message (with subchannels)			x	x	x				
Disconnect Part of Broadcast (without subchannels)				x	x				
Disconnect Part of Broadcast (with subchannels)			x	x	x				
Multipoint Connect/ Disconnect	x	x		x	x				
Bidirectional Connection	x	x		x	x				
Disconnect All									
Memory Dump (Connection and Data Memory)									x

The following table (**Table 3**) shows which parameter registers are considered by issuing an appropriate configuration command.

Table 3 Affected Registers for Configuration Commands

Command	Registers									
	CMD1	CMD2	SPA	ITSA	SCA	DPA	OTSA	GI1	GI2	TSV
Set H.1x0 Master/ Slave	x									
PLL Primary Master Ref.	x							x		
PLL Secondary Master Ref.	x							x		
PLL Source Selection	x									
H.100/H.110 Clock Output	x									
PCM Clock Output	x									
Comp. Clock Output	x									
CT_NETREF_1(2) Output	x									
H.100/H.110 Fallback	x									
Set Bit Rate Local Bus	x		x			x				
Set Bit Rate H.100/H.110	x		x							
Read Time Slot	x		x	x		x	x			
Stream to Stream Switch	x		x			x				
Clock Shift	x		x					x		
External Input Frequency		x								
Set Parallel Mode		x								
Set IREQ Pin		x								

Table 3 Affected Registers for Configuration Commands (cont'd)

Command	Registers									
	CMD1	**CMD2**	**SPA**	**ITSA**	**SCA**	**DPA**	**OTSA**	**GI1**	**GI2**	**TSV**
PCM and H.1x0 Standby		x								
Set Loop		x								
Frame Signal		x						x	x	
GPCLK Clock		x						x		
Set Range of Data Rate		x								
Read Configuration		x								x
Read GPCLK Configuration		x								x
Read PCM Line Configuration		x								x
Read H.1x0 Line Configuration		x								x
Read Bit Shift Configuration		x								x
Software Reset		x								

The command registers have the following structure:

7	6	5	4	3	2	1	0
I3	I2	I1	I0	CC3	CC2	CC1	CC0

CC3..0 is the command code and I3..0 is the parameter code.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEF	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 150	°C
Supply voltage	V_{DD}	– 0.5 to 4.6	V
I/O Supply voltage	V_{DD5}	– 0.5 to 7	V
Voltage on any input or output pin (referenced to ground)	VS	– 0.5 to VDD + 0.5 – 0.5 to VDD5 + 0.5	V
ESD robustness[1)] (HBM: 1.5 kΩ, 100 pF)	$V_{ESD,HBM}$	2000	V

1) According to MIL-Std. 883D, method 3015.7 and ESD Assoc. Standard EOS/ESD-5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

6.2 Operating Range

Table 5 Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Operating temperature	T_A	– 40	85	°C
Supply voltage	V_{DD}	3.13	3.47	V
I/O Supply voltage	V_{DD5}	4.75	5.25	V
Ground	V_{SS}	0	0	V
Voltage applied to input pins[1)]	V_{IN}	0	5.5	V
Voltage applied to output or I/O pins[2)] outputs enabled outputs high-Z	 V_{OUT} V_{OUT}	 0 0	 V_{DD} 5.5	 V V
Voltage applied to H.1x0 I/O pins in 3.3 V signal environment[3)] outputs enabled outputs high-Z	 VOUT VOUT	 0 0	 VDD VDD +0.3	 V V

1) If one of the H.1x0 input signals from the HTSI is used in 3.3 V and 5 V signal environment, the special VDD5 pins must be connected to 5 V as reference voltage to fulfill the operating range.

2) If one of the H.1x0 data ports and I/O signals or PCM16..31(IN/OUT) ports from the HTSI are used in 3.3 V and 5 V signal environment, the special VDD5 pins must be connected to 5 V as reference voltage to fulfill the operating range.

3) VDD5 is connected to 3.3 V

Note: In the operating range, the functions given in the circuit description are fulfilled.

6.3 Crystal Oscillator

The SWITI HTSI requires a 16.384 MHz or 32.768 MHz clock source. To supply this, a 16.384 MHz or 32.768 MHz crystal can be connected between the ECLKI and ECLKO pins. **Figure 20** shows the crystal with the external capacitors and resistors.

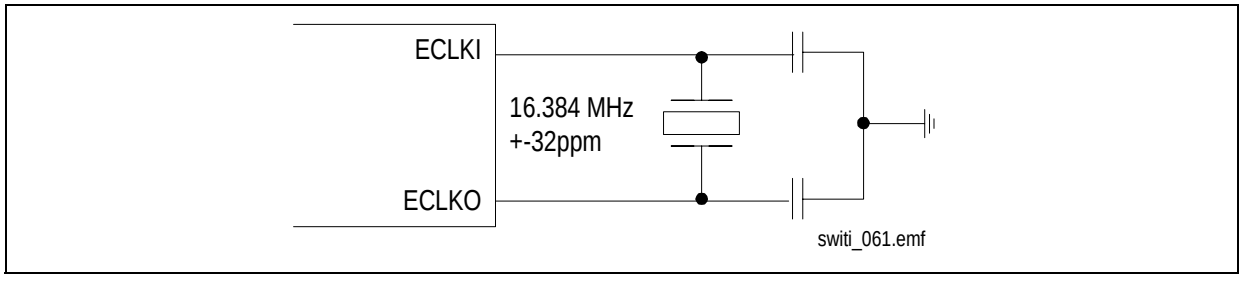


Figure 20 External Crystal

If a crystal is not used, a 16.384 MHz (± 32ppm or less) or a 32.768 MHz (± 32ppm) signal must be provided to the ECLKI pin and ECLKO should be left unconnected.

7 Package Outlines

P-PBGA-217-1
(Plastic Ball Grid Array Package)

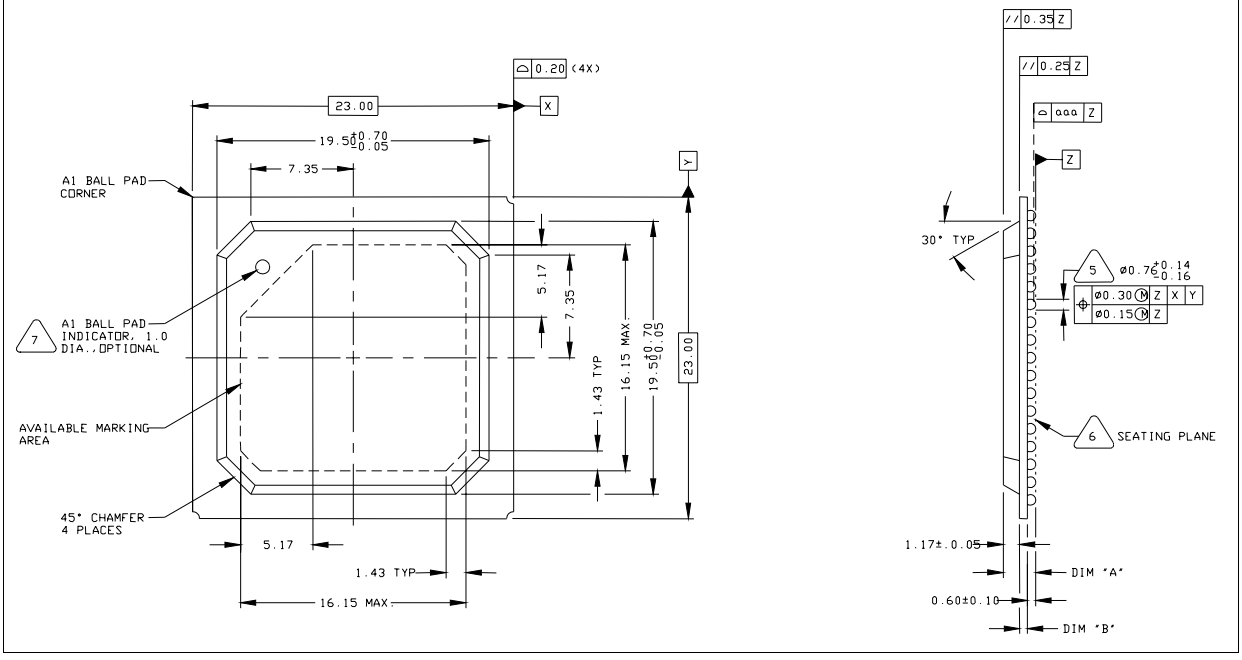


Figure 21 Outlines of P-PBGA-217-1

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

http://www.infineon.com

Published by Infineon Technologies AG